CLAIMS

1. A magnetic tunnel junction (MTJ) configuration for use in a magnetic memory cell, the configuration comprising:

a first free layer proximate to a first tunneling barrier;

a second free layer proximate to a second tunneling barrier and a pinned layer;

wherein the first free layer is sandwiched between the first and second tunneling layers.

2. The MTJ configuration of claim 1 wherein the first tunneling barrier has a magneto-resistance (MR) ratio that differs from a MR ratio of the second tunneling barrier.

3. The MTJ configuration of claim 1 wherein the first and second free layers comprise a synthetic anti-ferromagnetic structure.

4. The MTJ configuration of claim 1 further comprising:

a third free layer and a third tunneling layer;

wherein the second free layer is sandwiched between the second tunneling layer and the third tunneling layer.

5. The MTJ configuration of claim 1 further comprising

an anti-ferromagnetic layer, wherein the pinned layer is sandwiched between the first tunneling barrier and the anti-ferromagnetic layer.

6. The MTJ configuration of claim 1 wherein the pinned layer is a synthetic anti-ferromagnetic layer.

7. The MTJ configuration of claim 1 wherein the first tunneling barrier is comprised of a different material than the second tunneling barrier.

8. The MTJ configuration of claim 1 wherein the first tunneling barrier is formed from a different processing recipe than the second tunneling barrier.

9. The MTJ configuration of claim 1 wherein at least one of the free layers includes a single magnetic layer.

10. The MTJ configuration of claim 1 wherein at least one of the free layers includes a synthetic anti-ferromagnetic layer.

11. A magnetic memory cell comprising a switching element and a magnetic tunnel junction (MTJ) configuration comprising:

a first MTJ device including a first free layer, a first tunneling barrier, and a first pinned layer;

a second MTJ device including a second free layer, a second tunneling barrier, and a second pinned layer;

a first conductor connecting the first and second MTJ devices;

wherein a first magneto-resistance of the first MTJ device is different from a second magneto-resistance of the second MTJ device.

12. The memory cell of claim 11 wherein the second magneto-resistance is twice of the first magnetic resistance.

13. The memory cell of claim 11 wherein the second MTJ device includes an anti-ferromagnetic material and wherein the first free layer is connected to the anti-ferromagnetic material through the first conductor.

14. The memory cell of claim 11 wherein the MTJ configuration further comprises:

a second conductor connected to the second free layer;

wherein the first conductor connects to the first free layer and

wherein the first and second MTJ devices can be simultaneously written to using the second and first conductors respectively.

15. The memory cell of claim 11 wherein at least one of the free layers includes a spacer sandwiched between two ferromagnetic layers.

16. The memory cell of claim 11 wherein the first tunneling barrier is comprised of a different material than the second tunneling barrier.

17. The memory cell of claim 11 wherein the first tunneling barrier is formed from a different processing recipe than the second tunneling layer.

18. An integrated circuit comprising:

an input/output section;

a plurality of logic circuits connected to the input/output section; and

a plurality of magnetic memory cells connected to the logic circuits, the magnetic memory cells including a transistor and a storage structure including:

a first magnetic junction device including a first free layer, a first tunneling area, and a first pinned layer;

a second magnetic junction device including a second free layer, a second tunneling area, and a second pinned layer; and

a first conductor connected to configure the first and second magnetic junction devices in parallel.

19. The integrated circuit of claim 18 wherein a first magneto-resistance of the first magnetic junction device is different from a second magneto-resistance ratio of the second magnetic junction device.

20. The integrated circuit of claim 18 wherein the second magnetic junction device includes an anti-ferromagnetic material and wherein the first free layer is connected to the anti-ferromagnetic material through the first conductor.

21. The integrated circuit of claim 18 further comprising;

a second conductor connected to the second free layer;

wherein the first conductor connects to the first free layer; and

wherein the first and second magnetic junction devices can be simultaneously written to using the second and first conductors respectively.

22. The integrated circuit of claim 18 wherein at least one of the free layers includes a spacer sandwiched between two ferromagnetic layers.

23. The integrated circuit of claim 22 wherein the spacer comprises a synthetic anti-ferromagnetic material.

24. The integrated circuit of claim 18 wherein the first tunneling barrier is comprised of a different material than the second tunneling barrier.

25. The integrated circuit of claim 18 wherein the first tunneling barrier is formed from a different processing recipe than the second tunneling barrier.

26. The integrated circuit of claim 18 wherein a magneto-resistance ratio of the first tunneling barrier is 50-60% and a magneto-resistance ratio of the second tunneling barrier is 20-30%.